CLAIM LISTING

1-3. (Cancelled).

4. (Currently Amended) A unified memory system comprising:

a memory that is shared by a plurality of devices including at least a central processing unit and a graphics processing unit; ~~and~~

a memory request arbiter coupled to the memory, wherein the memory request arbiter performs real time scheduling of memory requests from different devices having different priorities, the unified memory system provides for real time scheduling of tasks, and provides access to memory by requesters that are sensitive to latency and do not have determinable periodic behavior;

dual memory controllers, the dual memory controllers including a first memory controller and a second memory controller, the memory request arbiter including a first arbiter coupled to the first memory controller and a second arbiter coupled to the second memory controller, wherein the first arbiter and the second arbiter perform real time scheduling of memory requests, wherein memory requests to the memory shared by the plurality of devices are routed to a particular one of the first arbiter and the second arbiter based on the address of the memory request; and

a memory select circuit receiving requests from the central processing unit and graphics processing unit, selecting one of the dual memory controllers and one of the first arbiter or second arbiter, and providing the request to the selected one of the dual memory controllers and the selected one of the first arbiter or second arbiter; and

wherein a predetermined minimum interval between subsequent accesses by a device is enforced, and wherein said predetermined minimum interval is long enough for another device to access.

5. (Previously Presented) The unified memory system of claim 4, wherein the central processing unit and the graphics processing unit are sensitive to latency and do not have determinable periodic behavior.

6. (Cancelled)

7. (Previously Presented) The unified memory system of claim 4 further comprising a circuit component associated with one or more devices and coupled between the associated devices and the memory request arbiter, wherein the circuit component is used to enforce at least a predetermined minimum interval between subsequent accesses by the associated device to the memory.

8. (Previously Presented) The unified memory system of claim 7 wherein the devices associated with the circuit component include a CPU.

9. (Previously Presented) The unified memory system of claim 7 wherein the devices associated with the circuit component make high priority service requests to access the memory through the circuit component.

10. (Previously Presented) The unified memory system of claim 7 further comprising a round robin server for

handling low priority tasks.

11. (Cancelled)

12. (Previously Presented) The unified memory system of claim 10, wherein the round robin server handles only low priority tasks.